Notice of Allowability	Application No.	Applicant(s)	
	09/783,246	HUTTON, MICHAEL D.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendments and actions filed 06/14/2006, 04/11/2006*.

2. ☒ The allowed claim(s) is/are *1-30*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date ____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. Claims 1-30 were examined.

Section I: Pre-Appeal Conference

2. This Office action has been prepared in response to the Pre-Brief Appeal Conference decision on 04/11/2006.

Section II: Interview

3. The Office instructed applicant, on 6/13/06, to provide amendments to the drawings and specification regarding abscent element numbers 412/414 from drawings and 514 from the specification to which applicant has agreed to.

Section III: Allowable Subject Matter

4. Claims 1-30 are allowable.

5. The following is an examiner's statement of reasons for allowance:

While US Patent 6,080,201 teaches (claim 1) a method of estimating a critical path delay during a source electric design into a target device, comprising: receiving an electronic representation of the source electronic design; determining a path criticality in the source electronic design based on, determining an actual delay corresponding to a connection already place across a first boundary in the target device, and determining a statistical estimate for a future delay corresponding to an associated future connection to be placed across a second boundary in the target device, wherein the statistical estimate for the future delay is made using estimates and partitioning at least a portion

of the source design by placing at least the portion of the source design across boundaries in the target device based on the determined actual delay and the statistical estimate for a future delay; (claim 19) a method for generating statistical estimates for future delays on uncut connections on a path in placing a design by partitioning methods comprising: receiving at least one source design; placing the at least one source design using partitioning methods to place the device across boundaries in the target device; US Patent 5,237,514 (claim 19) teaches generating statistic data corresponding to each type of boundary crossed in the target device, wherein the statistical data is generated using estimates; US Patent 6,367,056 teaches (claim 24) a computer program product comprising: a machine readable memory on which is provided program instructions for a method of placing a source electronic design code US Patent 6,080,201 teaches (claims 24 and 30) a computer system having a central processing unit (CPU) coupled to a memory, comprising: an interface for communicating with an individual; wherein the computer system is configured to receive an electronic representation of the source electronic design; wherein the computer system is configured to receive an electronic representation of the source electronic design; wherein the computer system is further configured to, determine a path criticality in the source electronic design based on determining an actual delay corresponding to a connection already placed across a first boundary in the target device, and determined a statistical estimate for a future delay corresponding to an associated future connection to be placed across a second boundary in the target device; and wherein the computer system is further configured to partition at least a

portion of the source design by placing the at least a portion of the source design across boundaries in the target device based on the determined actual delay; none of these references, taken either alone or in combination, with the prior art of record disclose

(claims 1 and 19) "of future cuts not made yet made in the target device,"

(claims 24 and 30) "associated with a future cut not yet made"

, in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicants' invention defines over the prior art of record.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Paul Rodriguez 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

June 15,2006

TS

Paul L. Rodriguez
Primary Examiner
Art Unit 2125